REMARKS

Claim 43 was rejected under 35 U.S.C. 102(a) as being anticipated by Bailey. This rejection is respectfully traversed. The Office Action states that Bailey shows non-conducting buried diffusion barrier of Si_3N_4, referring to column 13, line 31, and a second insulating layer 1176 of UTEOS. This is not correct. The Si_3N_4 layer referred to at column 13, line 31 is the layer 1186, which is not a buried layer and the capacitor is not located above this layer as claimed. The layer 1174 below the capacitor is a conducting layer. See, column 13, lines 1-3. Also it appears from the rest of the disclosure that the layer 1176 is not UTEOS, or if it is, the UTEOS is conducting. In FIG. 10B, the same layer is described as a "conductive barrier layer", and, in fact, if the layer 1176 was non-conducting, the device would not work because electricity could not go from the plug to the bottom electrode. Actually, those skilled in the art will recognize that the layer in which the numeral 1176 located is the UTEOS. It is likely that the draftsman should have underscored the numeral 1176 instead of using a lead line. Thus, for at least three reasons, Bailey does not anticipate claim 43.

Claims 44 – 56 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey in view of Asano et al. This rejection is respectfully traversed. Claims 44 – 48 are patentable at least because they depend on claim 43, which is patentable. In addition the Office Action recites at least one element of claim 44 that is not disclosed in any reference, claim 45 includes steps of removing portions of the third and second insulating layers to form an exposed portion of the buried diffusion barrier layer, claim 48 states that connection to the top plate-line electrode is remote from the capacitor stack, all of which are not in the references.

Claim 49 has been cancelled.

With respect to claim 50, the term top plate-line electrode has been changed to "thickened top-stack electrode", to more clearly distinguish it from the plate line 1192 of Bailey, which is a part of the metallization and not an electrode as the term is commonly used in the art. In the specification, the term top plate-line electrode was used to differentiate the initial thin electrode that was formed prior to patterning and the thicker electrode formed after patterning. Both however, clearly are part of the capacitor stack as

differentiated from a wiring layer 1192 that is separated from the capacitor stack. See, FIGS. 9 and 13 and the discussion thereof in the present application. However, that terminology is potentially confusing so it has been changed. None of the references disclose a process where a top stack-electrode is formed, the capacitor is patterned, and then the top stack-electrode is made thicker. Further, the claim now also includes the limitation that the initial top stack-electrode 100 nm or less thick. This is important because it is not physically possible to etch perfectly vertically. There is always a slope to the side wall. If the initial top stack-electrode is 100 nm or less, the slope of the capacitor side wall will be significantly less than if the full, thick electrode was originally formed. A sloped capacitor side wall reduces the capacitance for a given area of the base of the capacitor. This reduced capacitance reduces the robustness of the IC. The Office Action states with respect to claims 53 and 54 (which also claim the reduced size of the initial top stack-electrode) that the reduced thickness is obvious because it yields "sufficiently low resistivity". However, since the electrode is made thicker later, low resistivity is not the object here. The prior art does not disclose any reason for making the initial electrode so thin, so this is not obvious.

Claims 51 to 57 depend on claim 50, and are patentable for that reason at least. In addition, claims 52 and 55 recite a hard mask process, claims 53 and 54 recite thickness limitation, and claim 56 recites a planarizing, none of which are disclosed in the prior art in the context recited in the claims.

Claim 58 has been rejected on the basis that "annealing before or after patterning is a matter of design choice". This rejection is respectfully traversed. The Examiner has provided no support for this rejection. More importantly, the claim recites "crystallizing" after patterning the capacitor. Every one of the references of record in this application that discloses when crystallization takes place teaches crystallizing before patterning. See, for example, Kanaya et al. at paragraphs 84 – 88. The Examiner cannot say this is a design choice when no prior art reference ever taught such a choice.

Based on the forgoing amendments and arguments, claims 43 – 58 are believed to be in condition for allowance and their consideration and allowance is respectfully

requested. No additional fee is seen to be required. If any additional fee is seen to be required, please charge Deposit Account No. 50-1848.

Respectfully submitted,
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